REMARKS

The Examiner required that figures be submitted under 37 CFR 1.81. Accordingly, as the Examiner required Figures 1-3 are enclosed herewith for approval by the Examiner. These figures do not introduce new matter into the specification. All material in the drawings are based on disclosure of the invention as clearly present in the application as filed.

The disclosure has been amended as requested by the Examiner.

The claims have been amended as requested by the Examiner in order to include antecedent basis for "ink marking."

The claims have been amended to more particularly point out and recite the claimed invention. The claims as now submitted are now believed patentable over the prior art of record. The claims, as now presented specifically call for first encapsulating an integrated circuit dye into a package. The package is made of any acceptable material, such as ceramic, plastic or other encapsulation material. The completed package is introduced into a plasma chamber and a noble gas plasma, such as aragon, helium or the like. Actual atoms are removed from the package itself. After the removal of material from the package the package is removed from the plasma chamber and a pattern of ink markings apply to the package.

The present invention is distinctly different from any prior art or combination thereof. Applicants described in their own specification two prior art documents, one of which the Examiner now uses in the rejection. In particular, Applicants described and distinguished in their specification U.S. Patent Nos. 5,451,263 and 5,882,423 both to Linn see pages 2-4. These two prior art approaches have distinct disadvantages and draw backs from the claimed invention. The distinct disadvantagous of the '423 patent are the time and the residual chemical affects of using a florinated plasma. A florinated plasma takes substantial time, as can be seen and also involves substantial preparation and cleaning steps, none of which are necessary when a noble gas is used.

The Examiner was of the view that U.S. Patent to Arita et al. 6,418,941 was relevant to the claims of the present application. Applicants strongly disagrees. The Arita patent does not suggest or discuss an integrated circuit package. Instead, Arita is directed towards a technique for shielding the printed circuit board and leaving exposed the leads and an exposed

semiconductor dye during a cleaning process. There is no mention of plastic package or of the removal of material from an upper layer of a package. The present invention specifically states that material is physically removed from the package, which provides the claimed cleaning. Accordingly, the claims are believed patentable in light of Arita, '941, Linn, '423 or other prior art.

The Examiner also cited to Chang, U.S. Patent No. 5,043,299. The Chang patent is not seen has particularly relevant to the claimed invention, and is remarkably less relevant than the art which the inventor cited himself on pages 2-3 of the application as filed. Chang et al deals with normal semiconductor processing techniques and the making of the wafer having integrated circuits thereon. There is nothing in Chang et al. to teach or suggest the use of a noble type gas for the removal of an upper layer package which contains on the inside thereof an integrated circuit dye.

The Director is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

All of the claims remaining in the application are now clearly allowable. Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,

SEED Intellectual Property Law Group PLLC

David V. Carlson
Registration No. 31,153

DVC:lcs
Enclosures:
Postcard
Formal Drawings (Figs. 1-3)

701 Fifth Avenue, Suite 6300
Seattle, Washington 98104-7092
Phone: (206) 622-4900
Fax: (206) 682-6031
421075_1.DOC